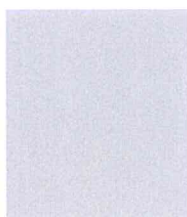


PERSONAL INFORMATION

Andrea Severino



95025, Italy

+39 095 +39

andrea.severino@st.com

[State personal website\(s\)](#)

Sex : Male

Date of birth 07/05/1980

Nationality Italian

Enterprise	University	EPR
<input type="checkbox"/> Management Level	<input type="checkbox"/> Full professor	<input type="checkbox"/> Research Director and 1st level Technologist / First Researcher and 2nd level Technologist
<input checked="" type="checkbox"/> Mid-Management Level	<input type="checkbox"/> Associate Professor	<input type="checkbox"/> Level III Researcher and Technologist
<input type="checkbox"/> Employee / worker level	<input type="checkbox"/> Researcher and Technologist of IV, V, VI and VII level / Technical collaborator	<input type="checkbox"/> Researcher and Technologist of IV, V, VI and VII level / Technical collaborator

WORK EXPERIENCE

From 2018

R&D section manager – Growth and advanced characterization of WBG materials

St Microelectronics Catania

- GaN, SiC and Si substrate and epitaxy evaluation
- Material Characterization

STMicroelectronics ADG-R&D

From 2012-2018

R&D process engineer

St Microelectronics Catania

- GaN, SiC and Si substrate and epitaxy evaluation
- Oxide and thermal processes
- Material Characterization

EDUCATION AND TRAINING

2008-2012

Post Doc Position at IMM-CNR, Catania

IMM-CNR, Catania

- Heteroepitaxy of SiC on Si substrate
- Material Characterization

2005-2008

Ph D in Material Science at University of Catania

1998-2004

Master Degree in Physics at University of Catania

PERSONAL SKILLS

Mother tongue(s) Italian

Other language(s) **Fluent written and oral English**

Job-related skills **Expertise in Material Science, Good team worker**

Digital skills **Several software**

Other skills

ADDITIONAL INFORMATION

Publications

[PROCESS FOR MANUFACTURING A SILICON CARBIDE SEMICONDUCTOR DEVICE HAVING IMPROVED CHARACTERISTICS](#)
N Piluso, A Severino, S Rinaldi Beatrice, A Mazzeo, L Caudo, A Russo, ...
US Patent App. 17/368,437

[Status of 3 C-SiC Growth and Device Technology](#)
P Wellmann, M Schöler, P Schuh, M Jennings, F Li, R Nipoti, A Severino, ...
Wide Bandgap Semiconductors for Power Electronics: Materials, Devices ...

[Effect of interface and bulk charges on the breakdown of nitrided gate oxide on 4H-SiC](#)
B Mazza, S Patané, F Cordiano, M Giliberto, G Renna, A Severino, ...
2021 IEEE International Reliability Physics Symposium (IRPS), 1-4

[Active dopant profiling and Ohmic contacts behavior in degenerate n-type implanted silicon carbide](#)
M Spera, G Greco, A Severino, M Vivona, P Fiorenza, F Giannazzo, ...
Applied Physics Letters 117 (1), 013502

[Impact of threading dislocations detected by KOH etching on 4H-SiC 650 V MOSFET device failure after reliability test](#)
A Severino, R Anzalone, N Piluso, E Vitanza, B Carbone, A Russo, ...
Materials Science Forum 1004, 472-476

[An Approach to Predict 4H-SiC Wafer Bending after Back Side Thinning by Substrate Resistivity Analysis](#)
N Piluso, S Rinaldi, S Lorenti, A Bassi, A Severino, S Coffa
Materials Science Forum 1004, 57-62

[HEMT transistors with improved electron mobility](#)
F Iucolano, A Severino, MC Nicotra, A Patti
US Patent 10,396,192

[Effect of high temperature annealing \(T> 1650 C\) on the morphological and electrical properties of p-type implanted 4H-SiC layers](#)
M Spera, D Corso, S Di Franco, G Greco, A Severino, P Fiorenza, ...
Materials Science in Semiconductor Processing 93, 274-279

[Ohmic contacts on p-Type Al-Implanted 4H-SiC layers after different post-implantation annealings](#)
M Spera, G Greco, D Corso, S Di Franco, A Severino, AA Messina, ...
Materials 12 (21), 3468

MAX 2 PAGINE

MAX 10 pubblicazioni pertinenti le tematiche di interesse negli ultimi 10 anni

